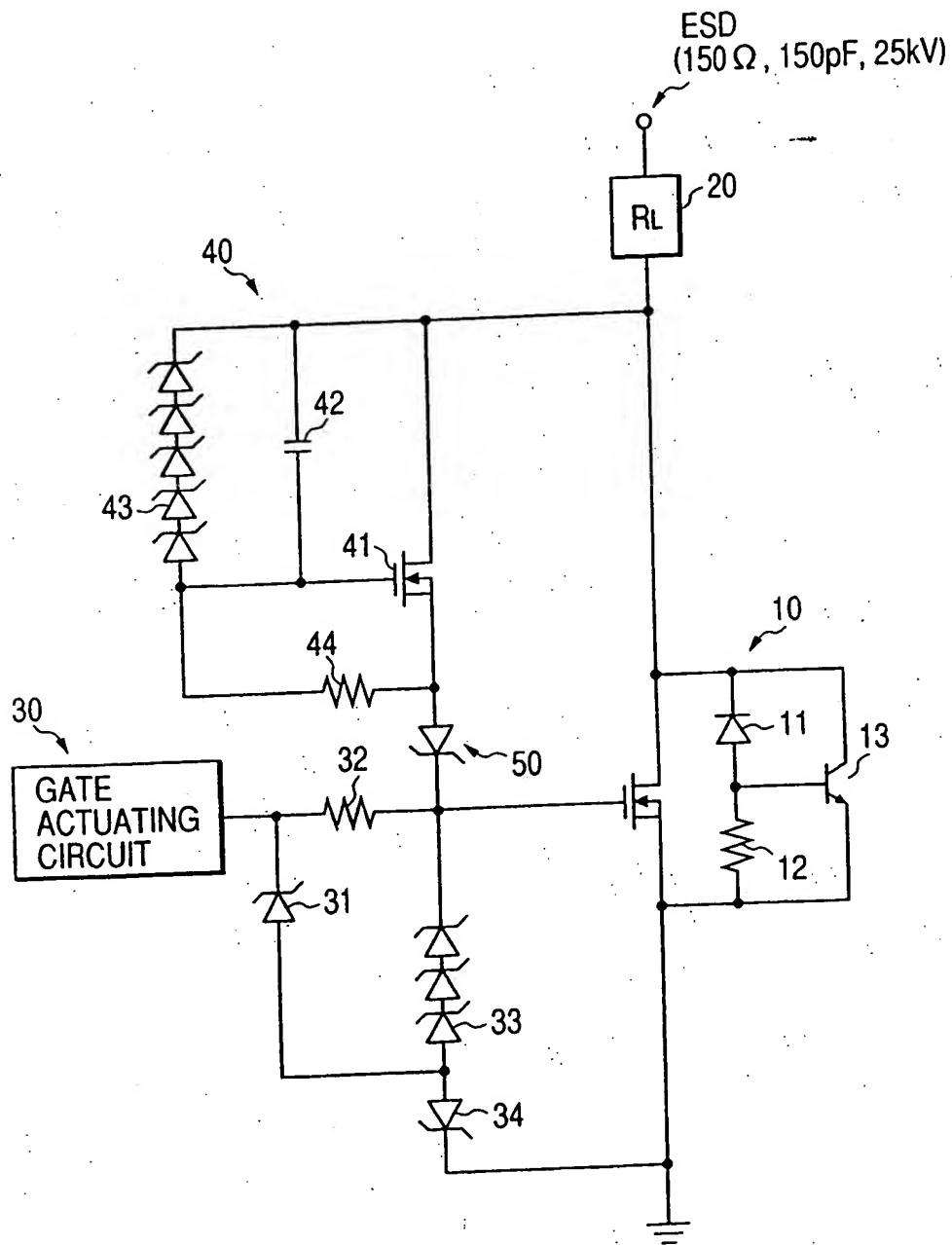




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FIG. 1



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FIG. 2A

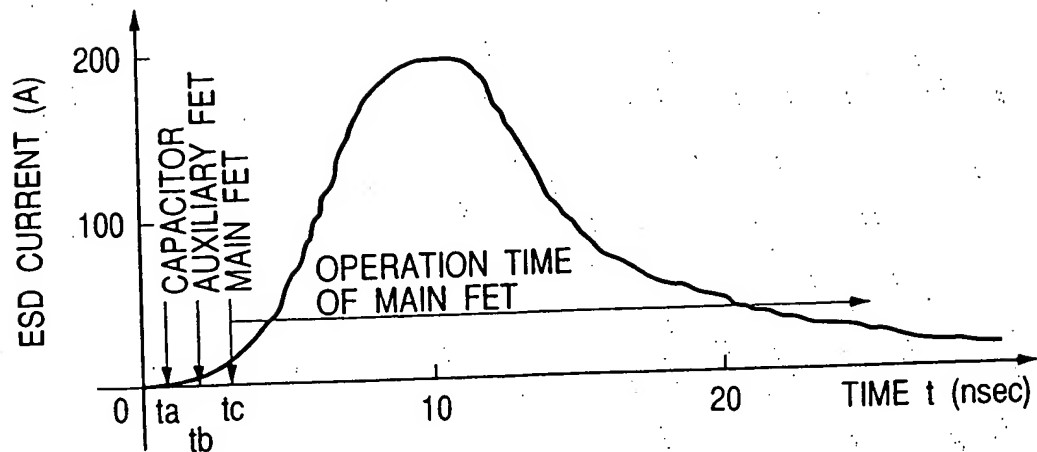
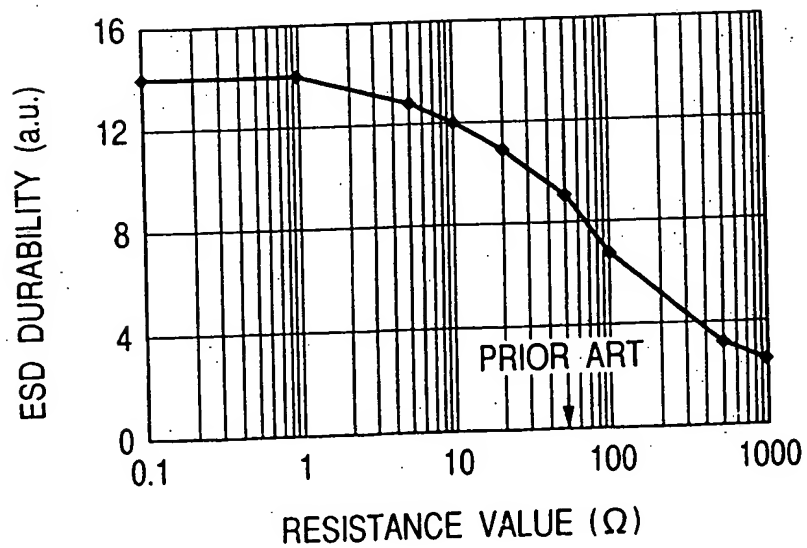


FIG. 2B



The diagram shows a gate actuating circuit 30 connected to the gate of a MOSFET 10. The MOSFET 10 has its source connected to ground and its drain connected to a load RL 20. A protection circuit 60 is connected between the gate and the drain. This circuit includes a resistor 62a and a capacitor 62b in parallel, with a diode 61 in series with the capacitor. The gate is also connected to a diode 50 and a resistor 32, which are in parallel with each other and with the gate of the MOSFET 10. The diode 50 is oriented with its cathode towards the gate and its anode towards the drain. The MOSFET 10 is shown with its internal structure, including a gate 11, a drain 12, and a source 13.

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FIG. 4

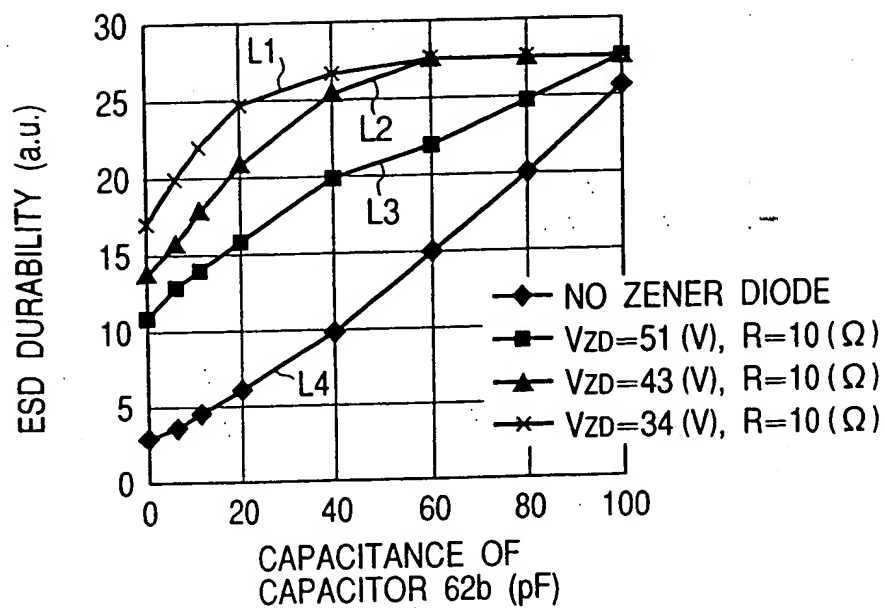
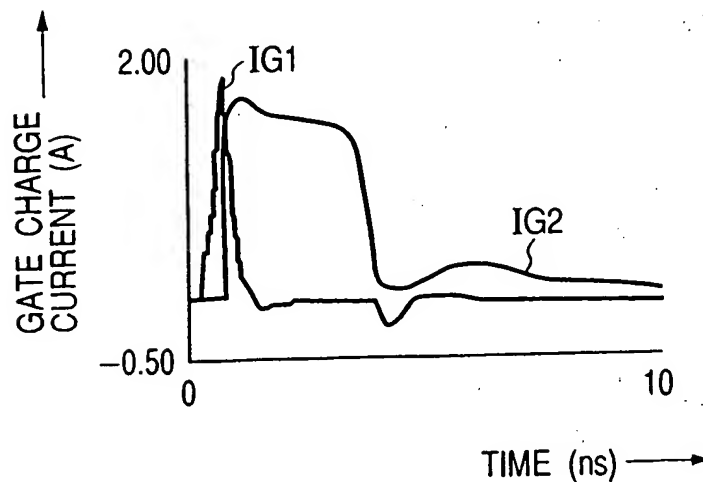
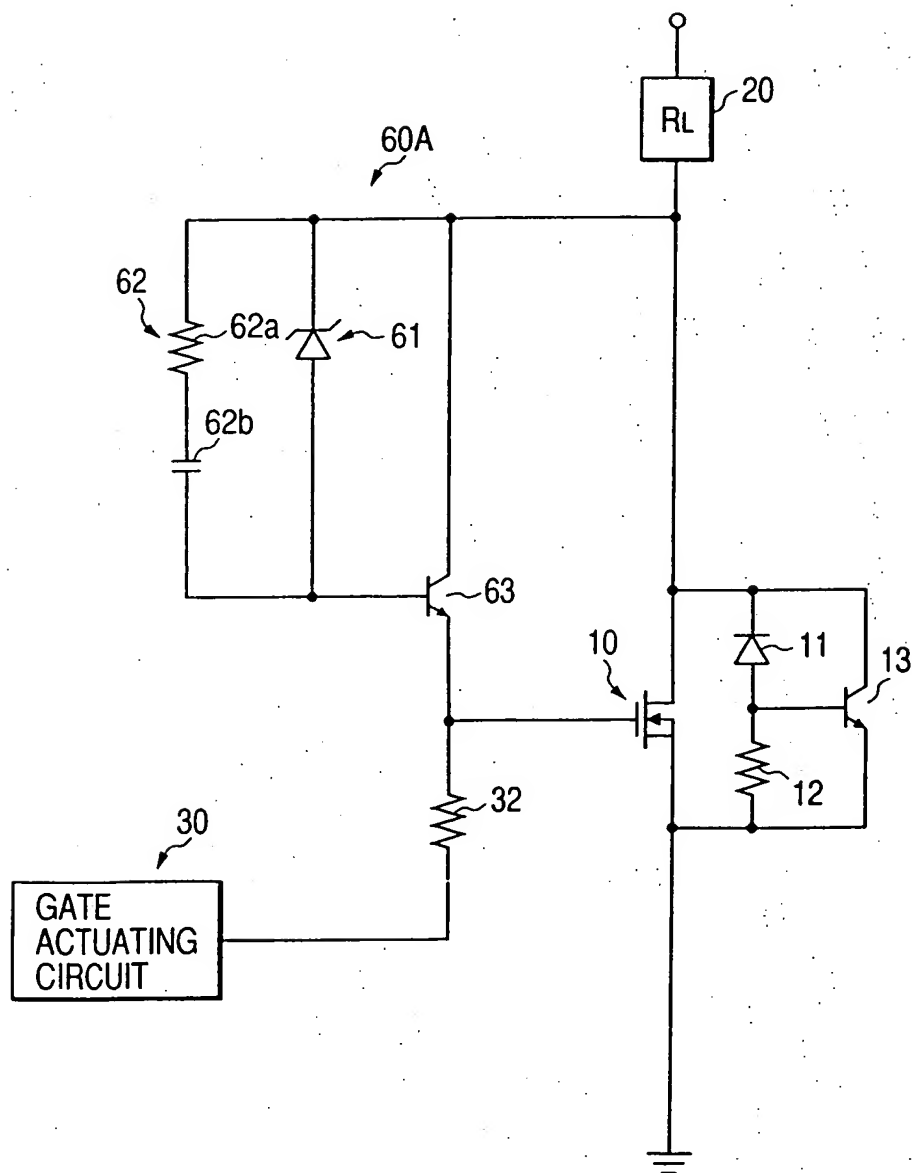


FIG. 5



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FIG. 6



The diagram shows a multi-stage driver circuit. A load RL (20) is connected to a common output node. The circuit includes a series of transistors (71, 72, 73) and resistors (75, 76, 77, 78) forming a current source or divider network. A gate actuating circuit (30) is connected to the gates of the transistors. A diode (50) and a resistor (32) are connected to the output node. A feedback loop (10) is formed by a diode (11) and a resistor (12) connected to the output node and ground. A transistor (13) is also connected to the output node and ground.

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FIG. 8

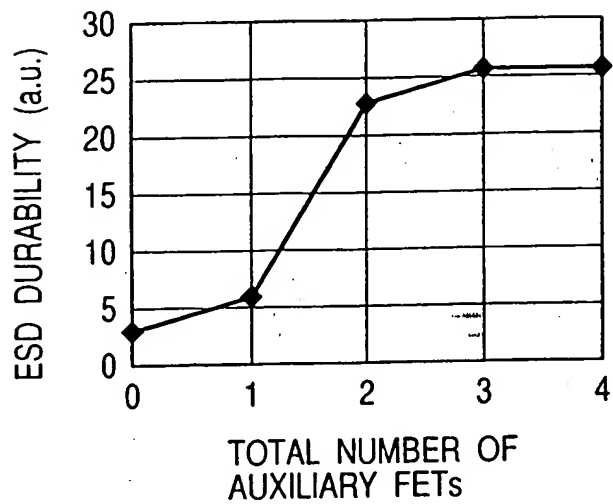


FIG. 10

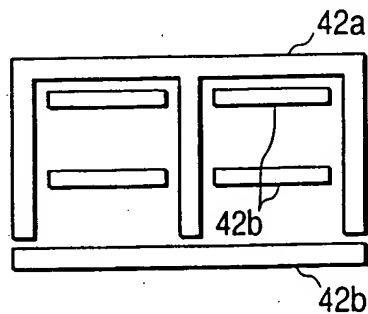
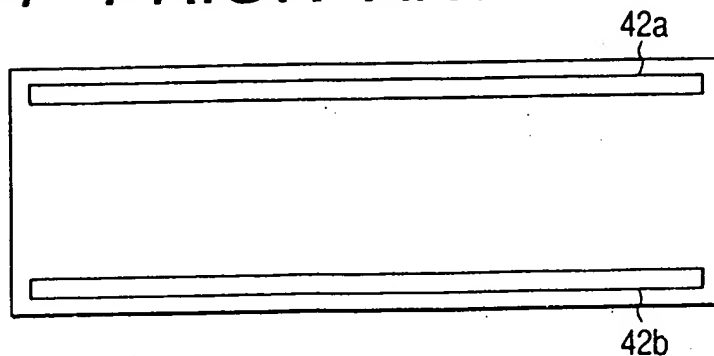
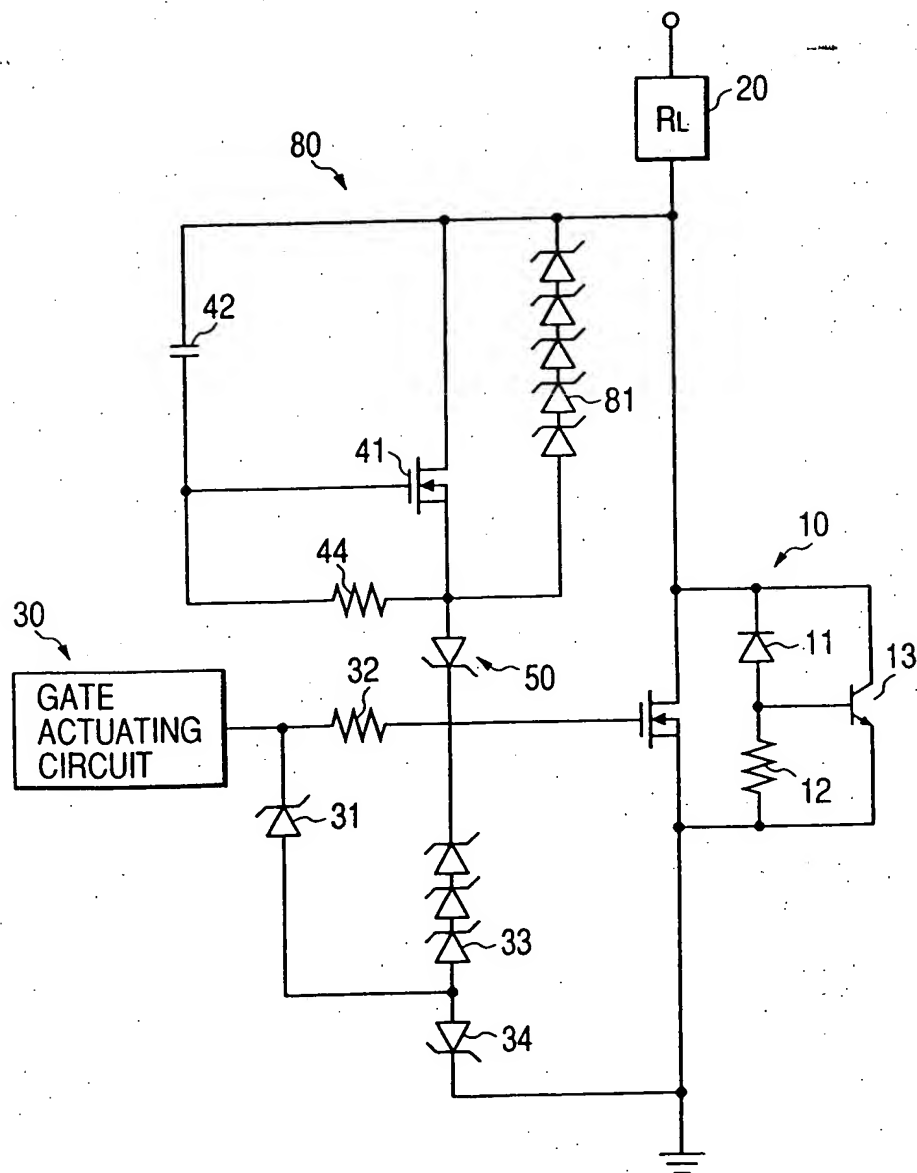


FIG. 11 PRIOR ART



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FIG. 9



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FIG. 12A

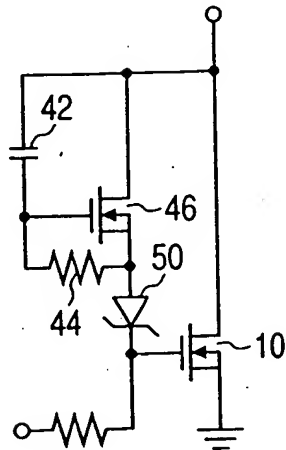


FIG. 12B

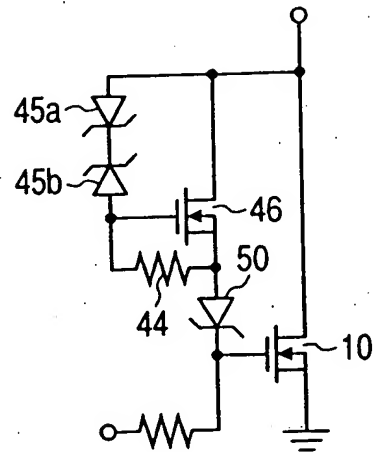


FIG. 14

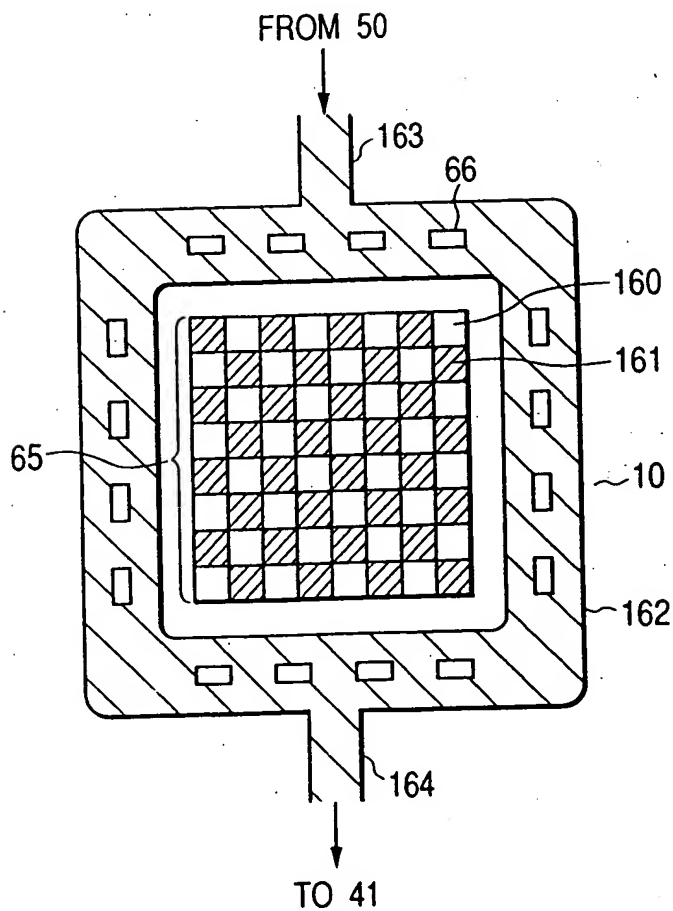


FIG. 1 is a plan view of a semiconductor chip. The chip contains a central array of FETs 10. Each FET 10 has a drain 42 and a source 50. The array is surrounded by pads 13b. Labels include CHIP, PAD, 42, FET 46, DRAIN, SOURCE, 50, 13b, and FET 10.

[illegible]

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FIG. 15A

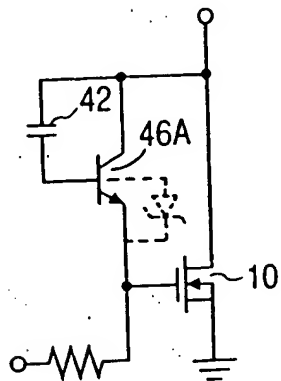


FIG. 15B

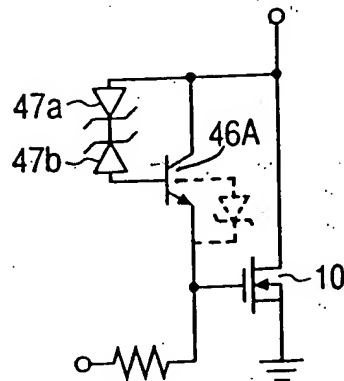


FIG. 16A

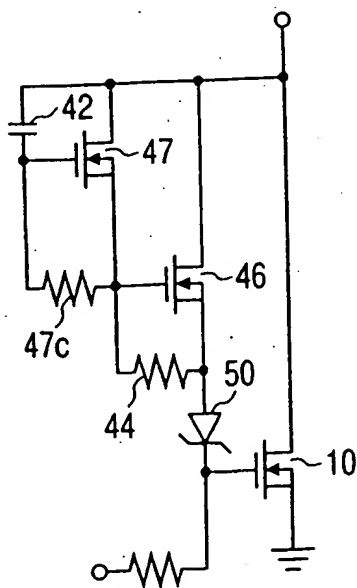
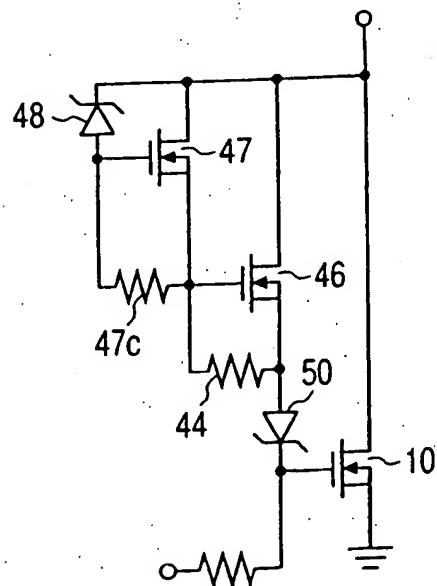


FIG. 16B



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FIG. 17A

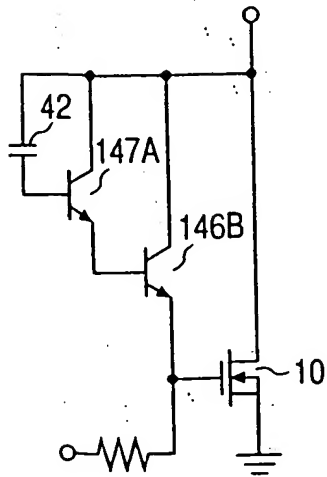


FIG. 17B

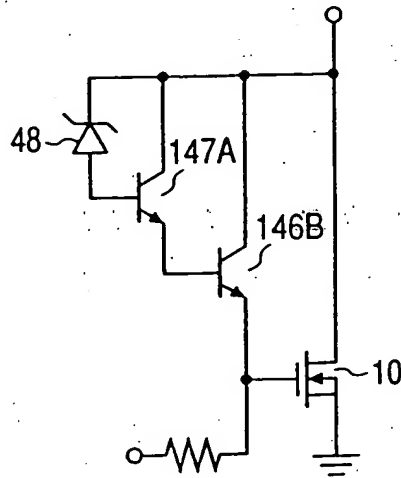


FIG. 18A

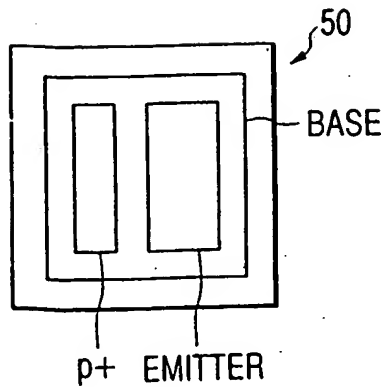
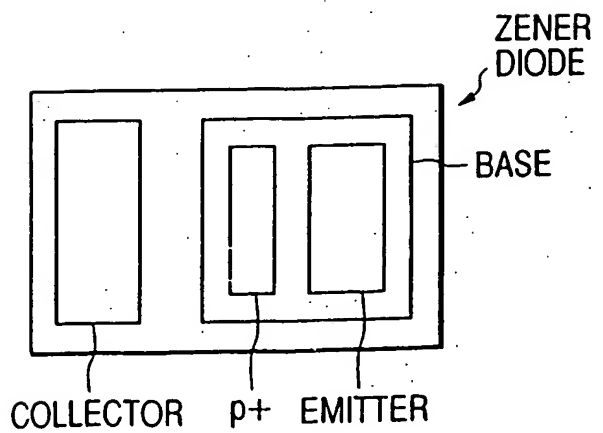
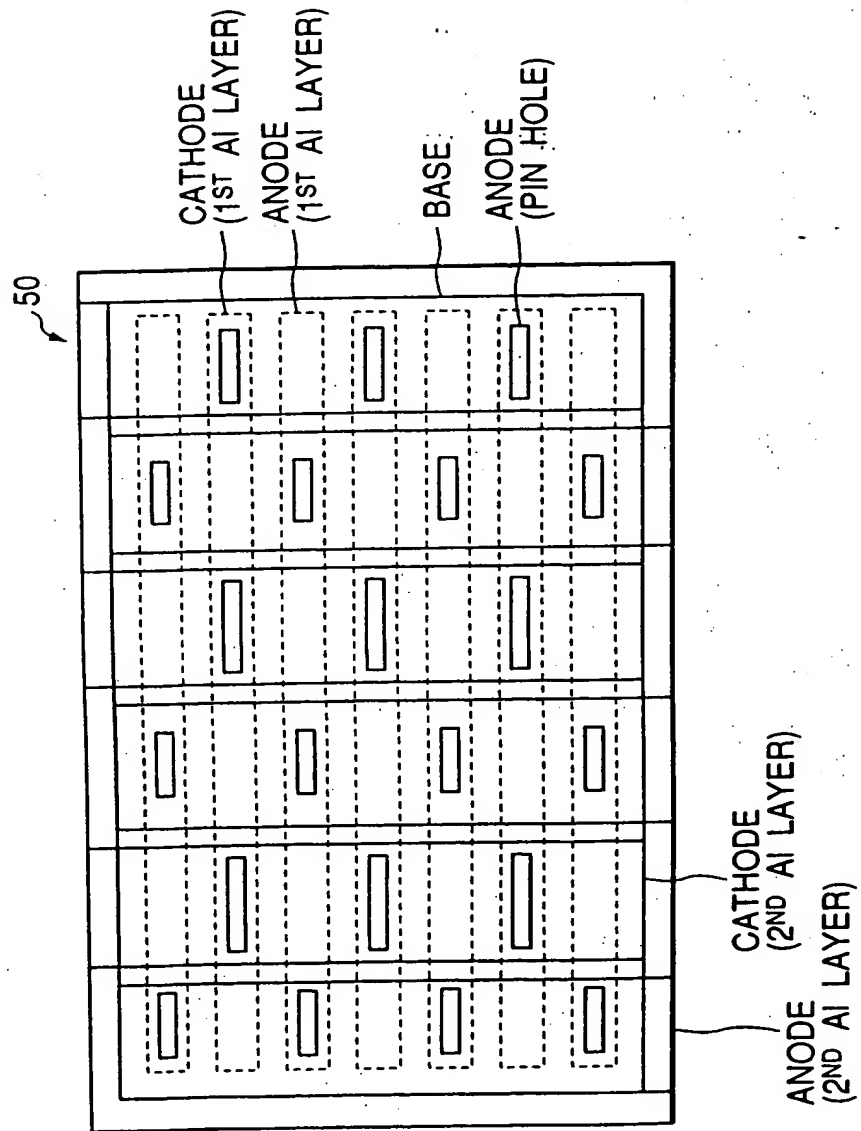


FIG. 18B
PRIOR ART



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FIG. 19



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FIG. 20A

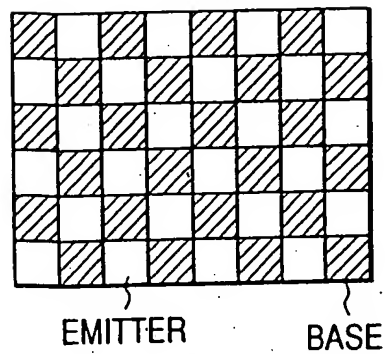


FIG. 20B

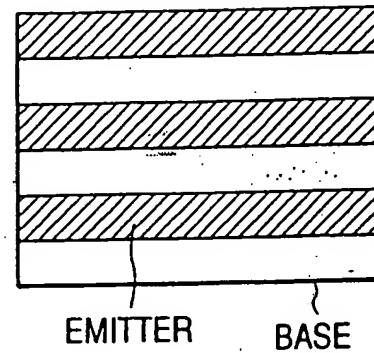
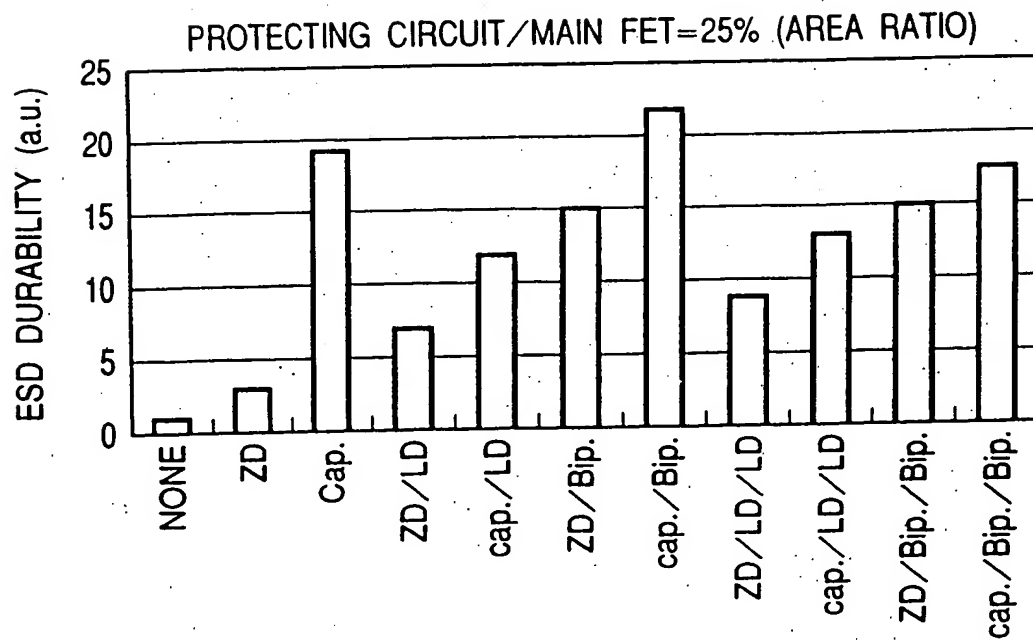
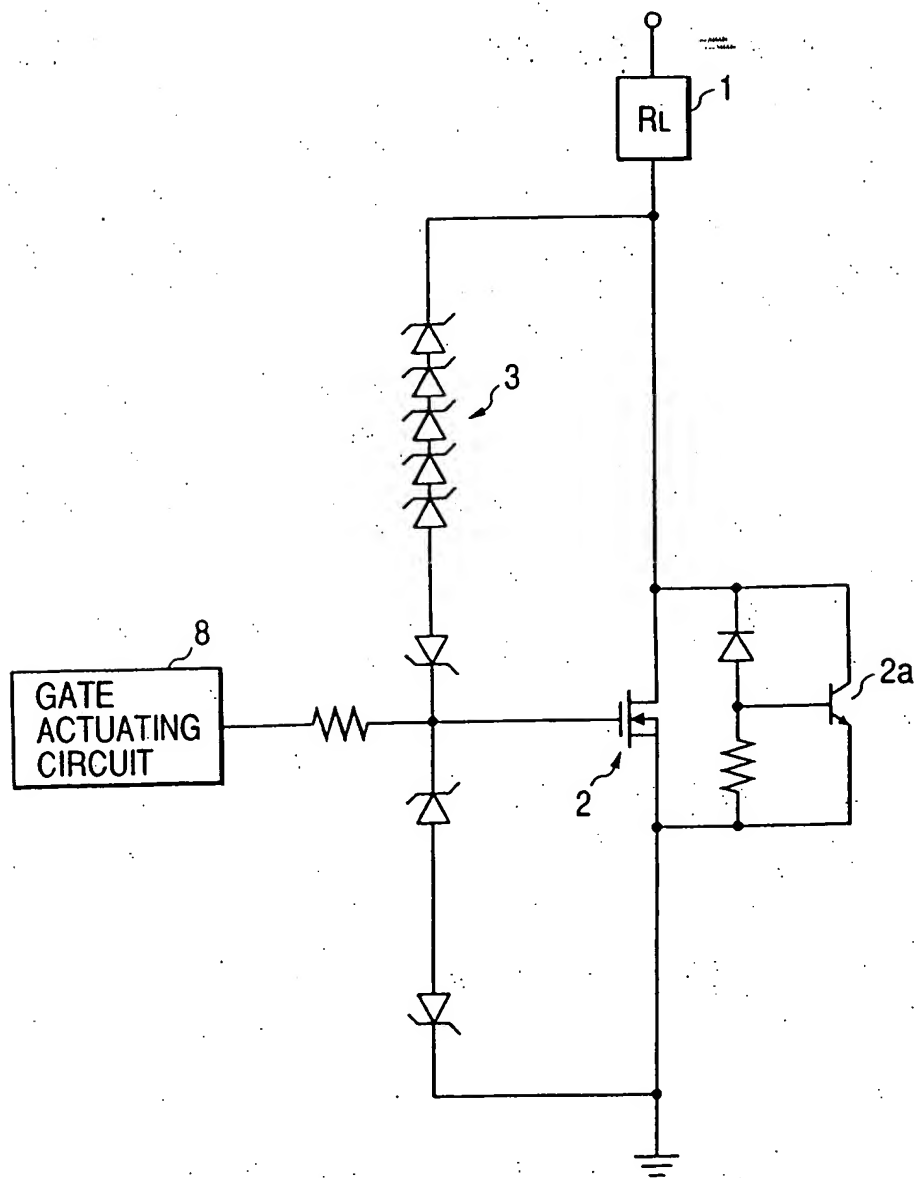


FIG. 21



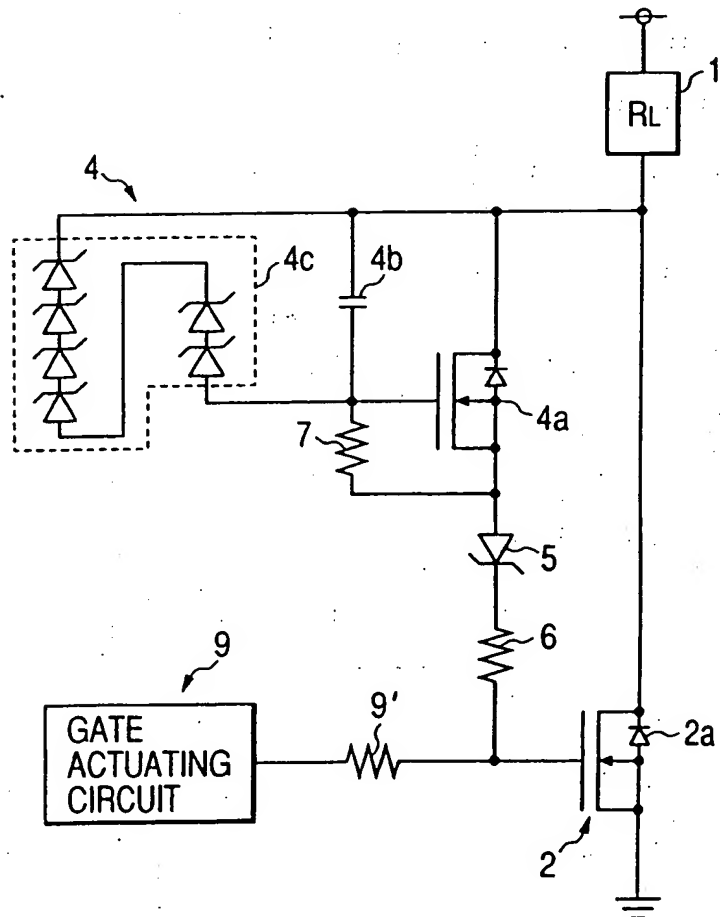
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FIG. 22 PRIOR ART



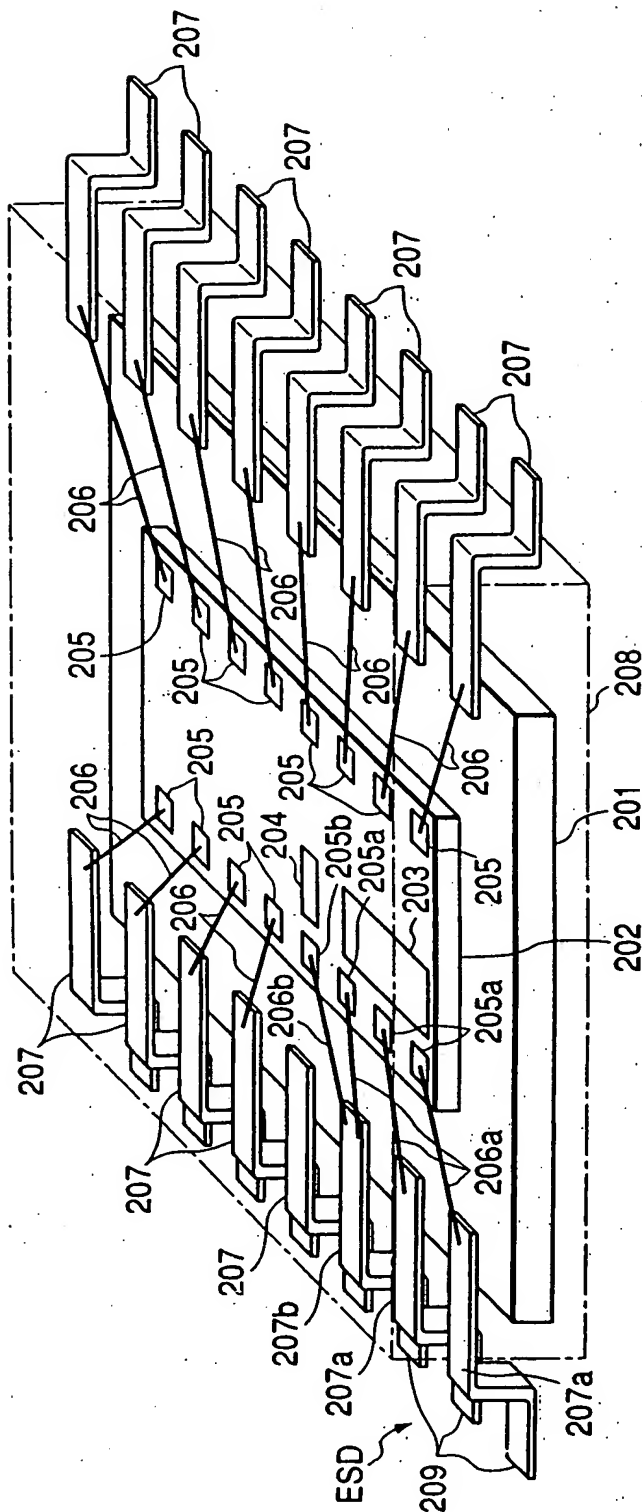
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FIG. 23 PRIOR ART



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FIG. 24

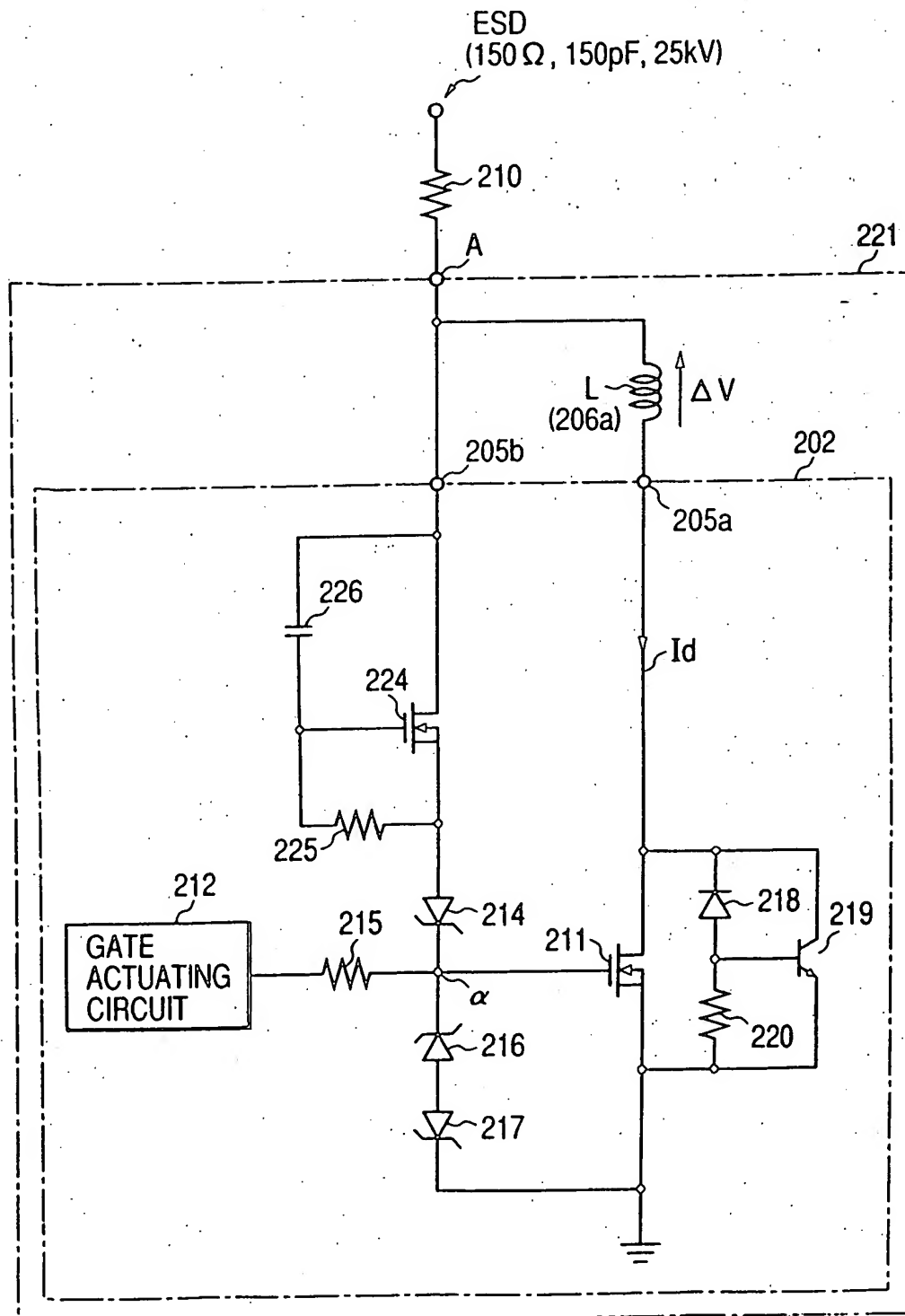


[illegible]

[illegible]

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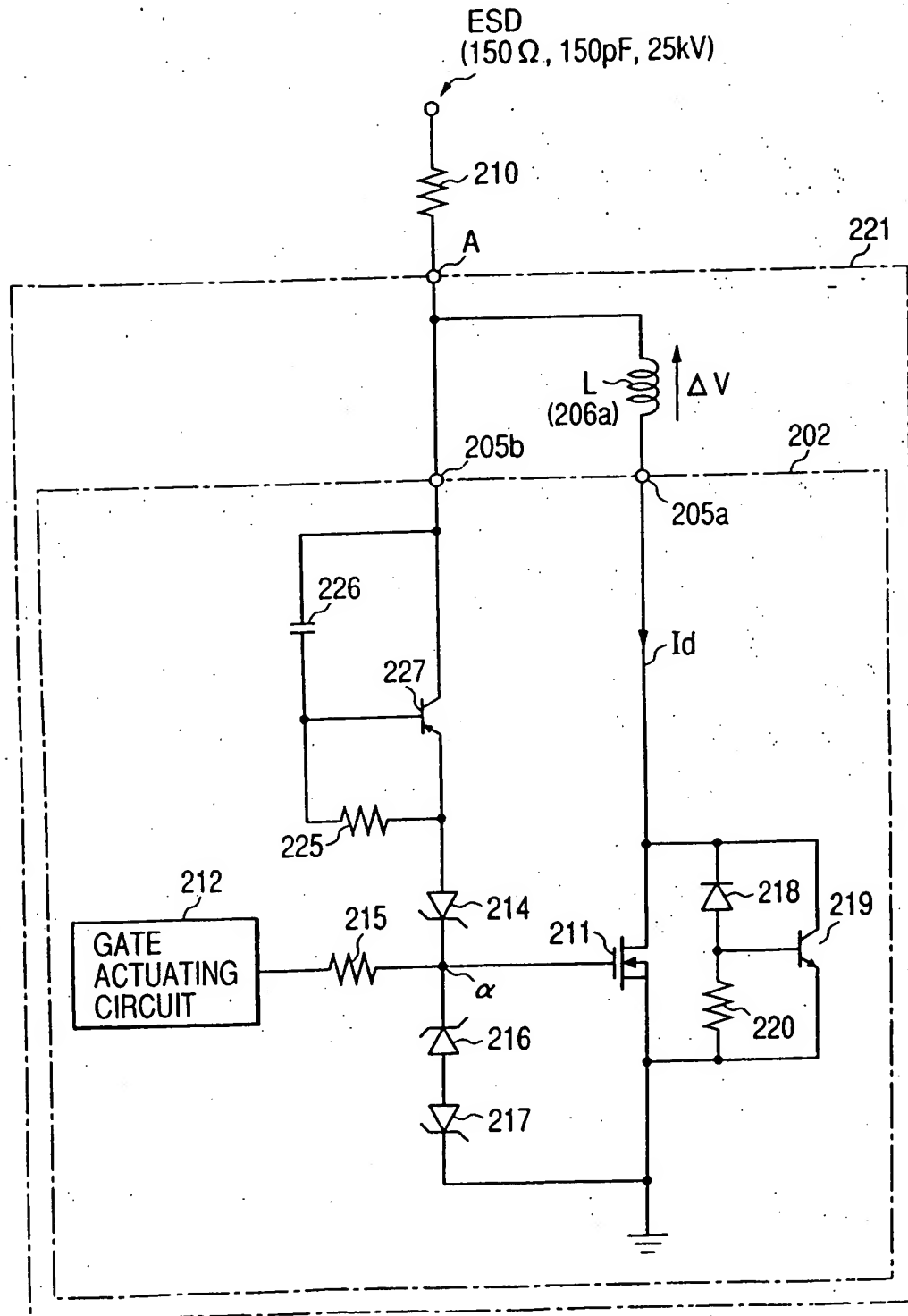
FIG. 27



The diagram shows a semiconductor device with an ESD protection circuit. An ESD source (150 Ω , 150 pF, 25 kV) is connected to a resistor 210, which leads to a node A. Node A is connected to a vertical line containing a series of diodes 223, 227, and 225. A resistor 225 is connected to the node between diodes 227 and 225. A gate actuating circuit 212 is connected to a resistor 215, which is connected to a node between diodes 214 and 216. Diodes 214, 216, and 217 are connected in series to ground. A transistor 211 has its gate connected to the node between 214 and 216, its source to ground, and its drain to a node 205a. Node 205a is connected to a vertical line containing a diode Id and a resistor 220. A transistor 219 has its gate connected to node 205a, its source to ground, and its drain to a node 205b. Node 205b is connected to a vertical line containing a resistor 210 and a node A. A coil L (206a) is connected between node 205b and node 202. A voltage ΔV is indicated across the coil L. The entire circuit is enclosed in a dashed box 221.

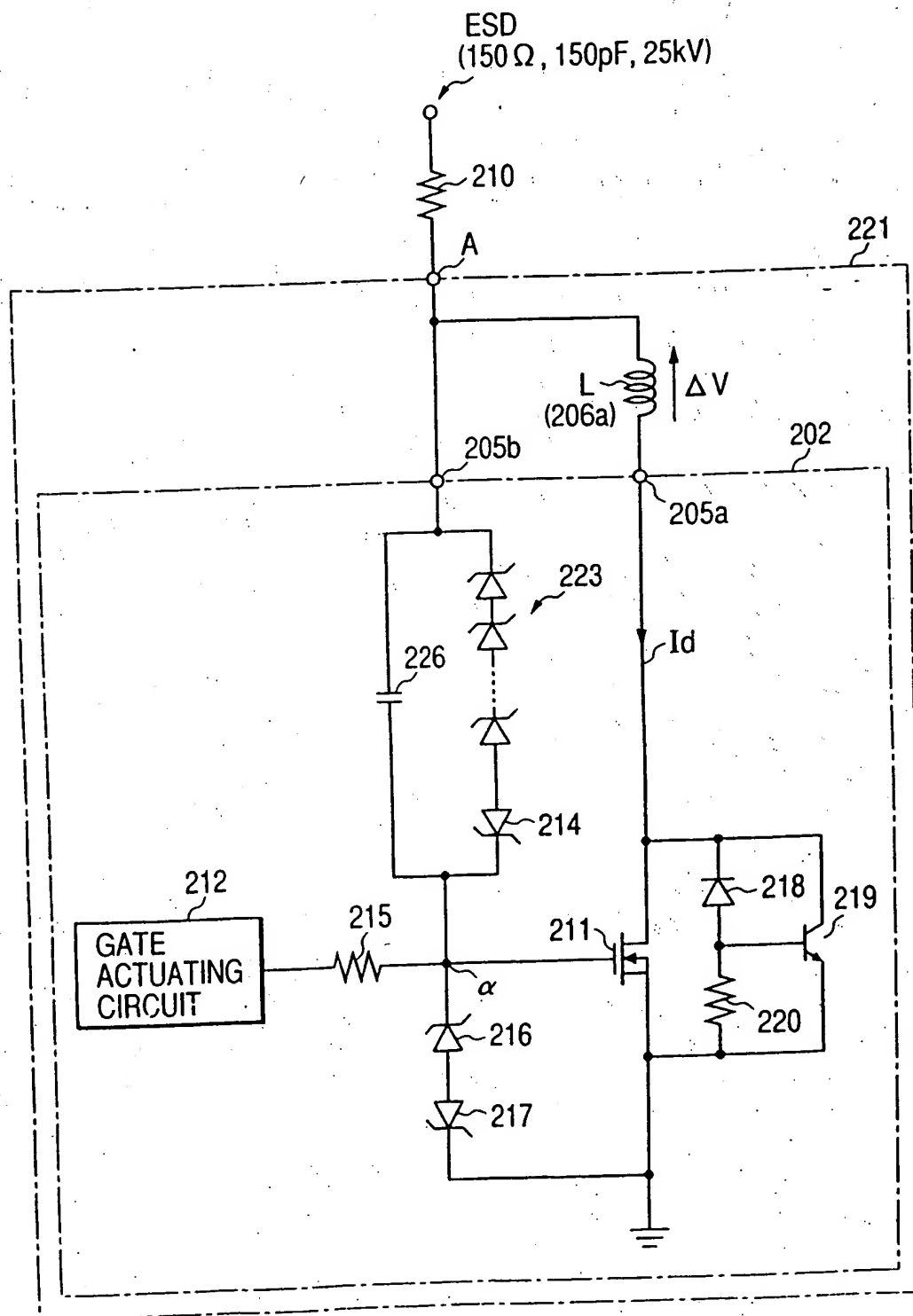
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FIG. 29



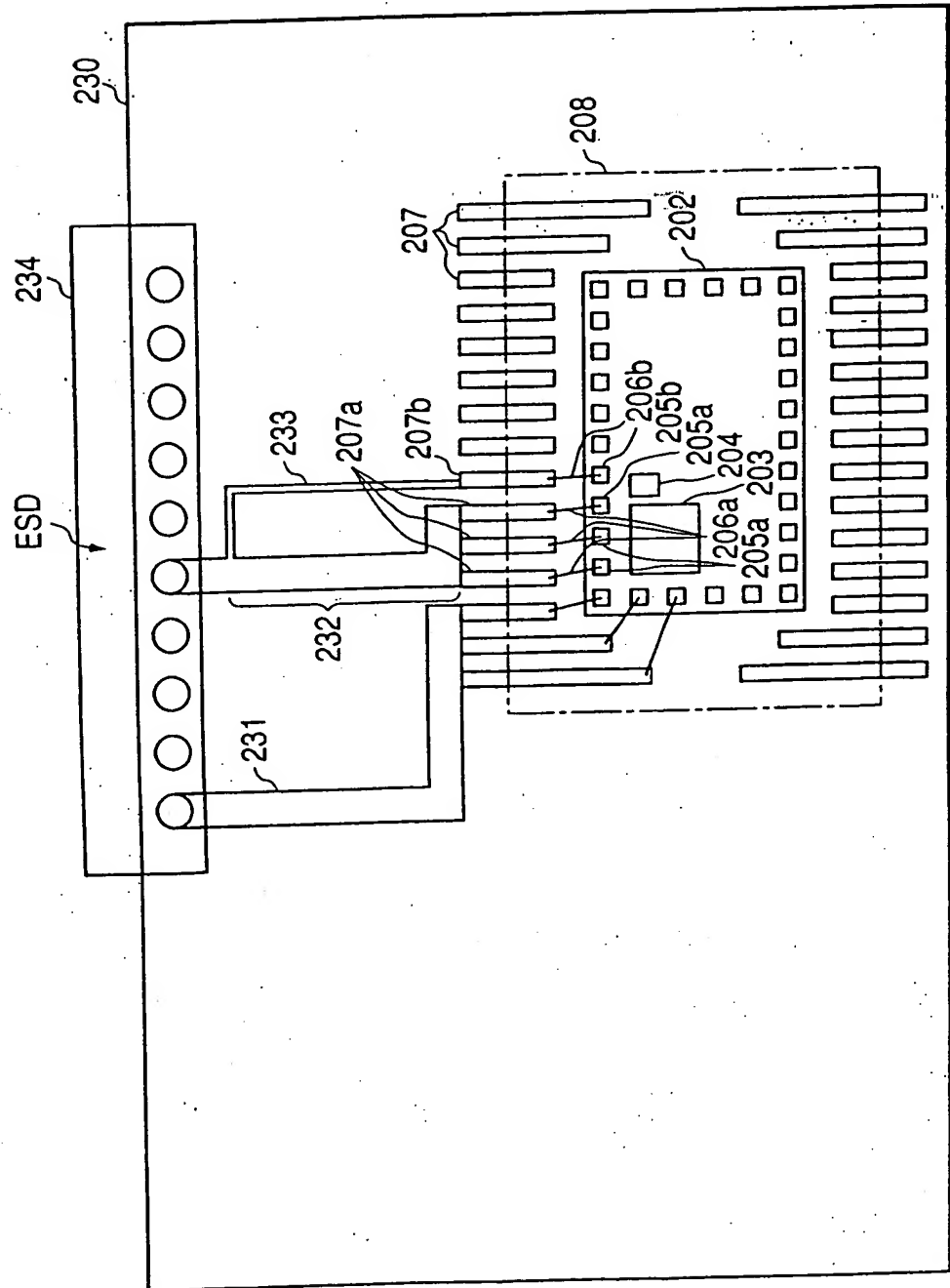
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FIG. 30



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FIG. 31



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FIG. 32A

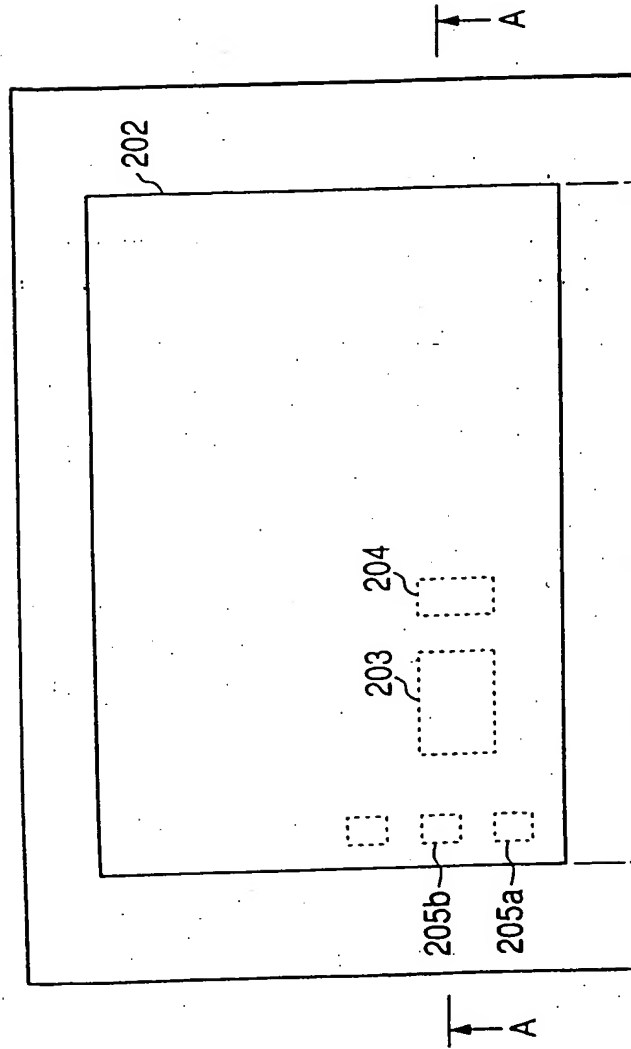
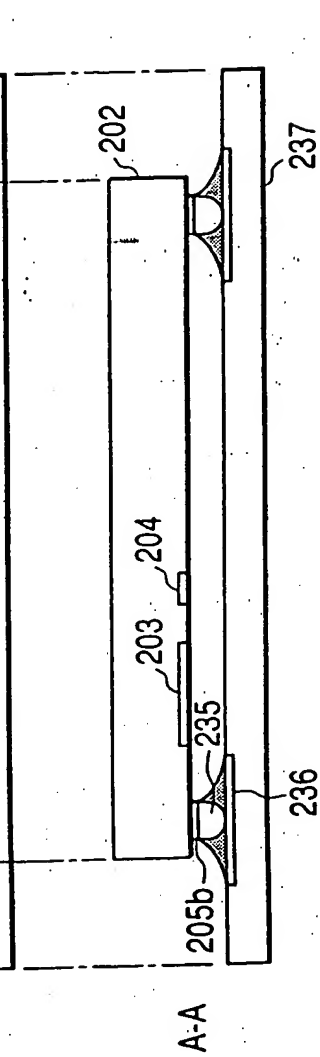
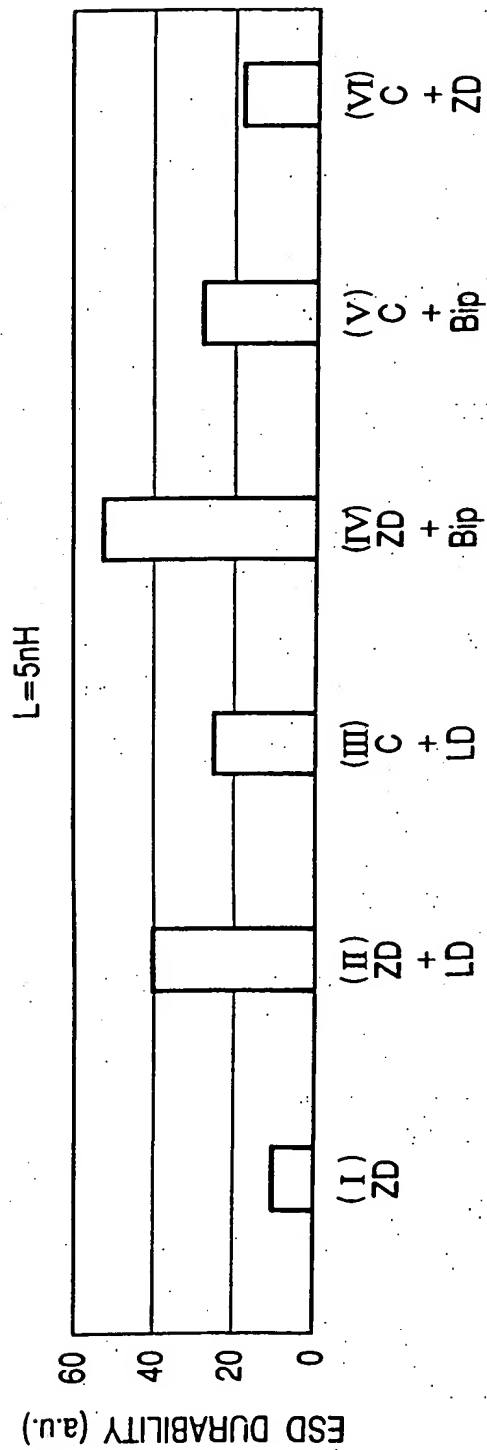


FIG. 32B



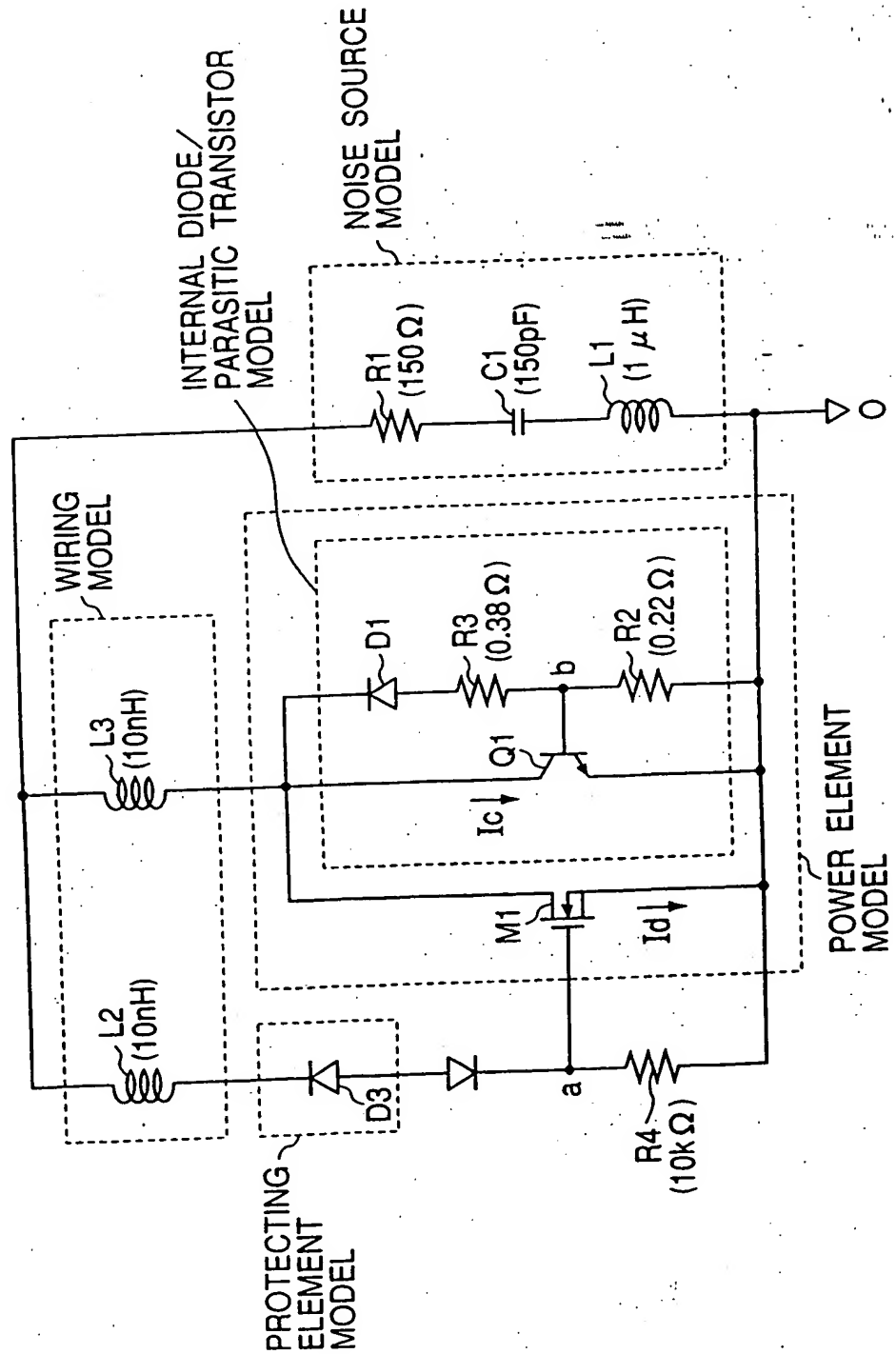
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FIG. 33



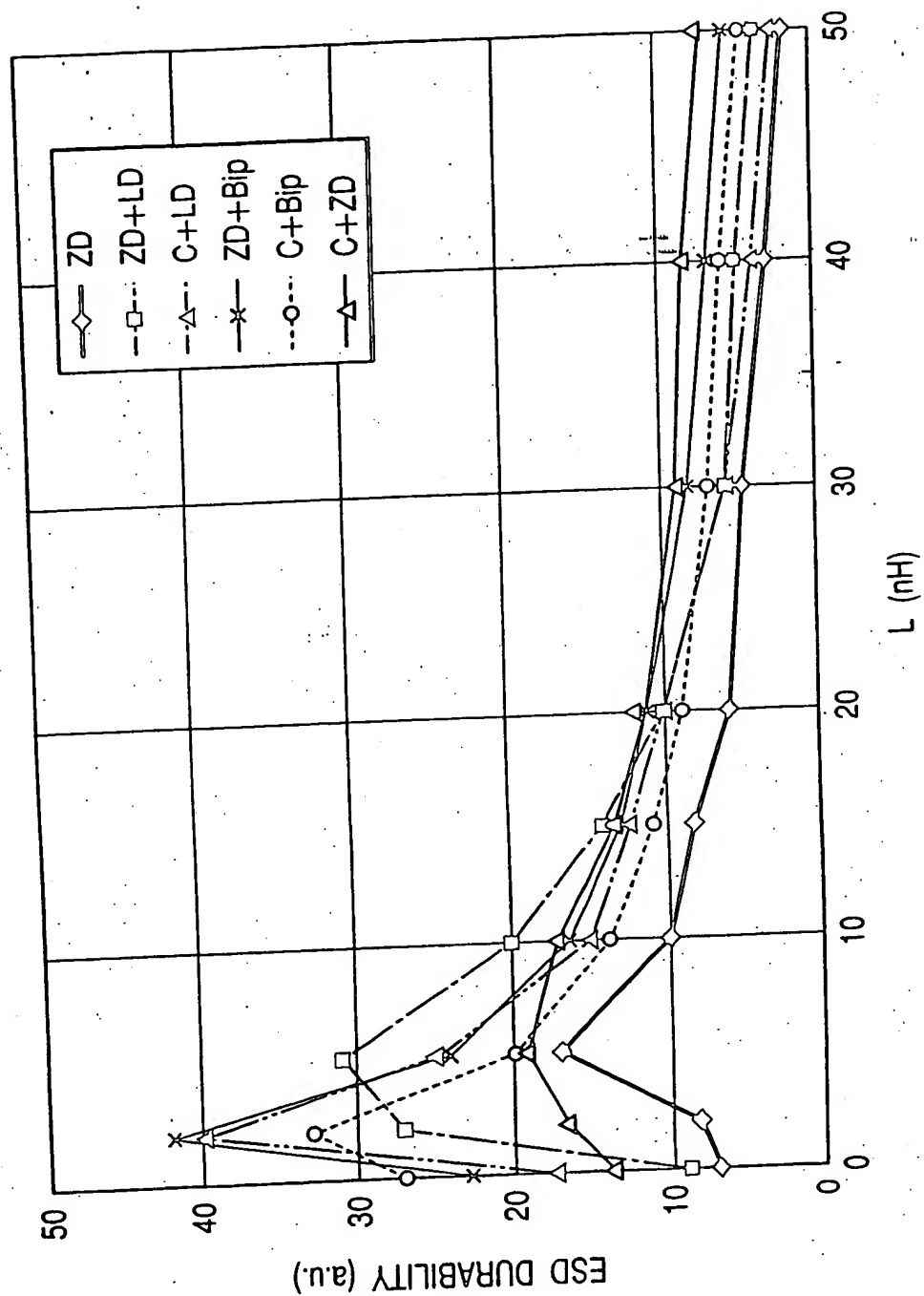
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FIG. 34



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FIG. 35



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FIG. 36A

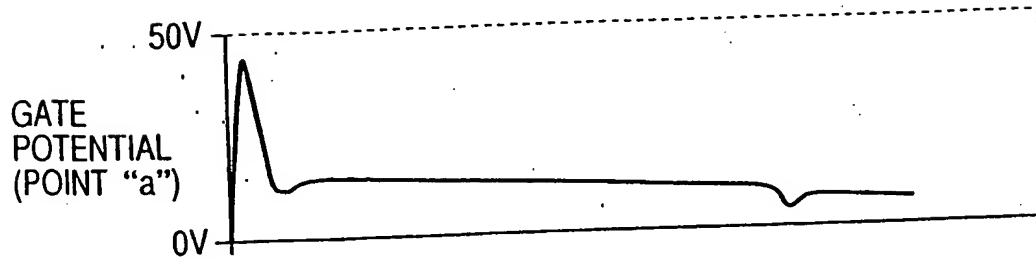


FIG. 36B

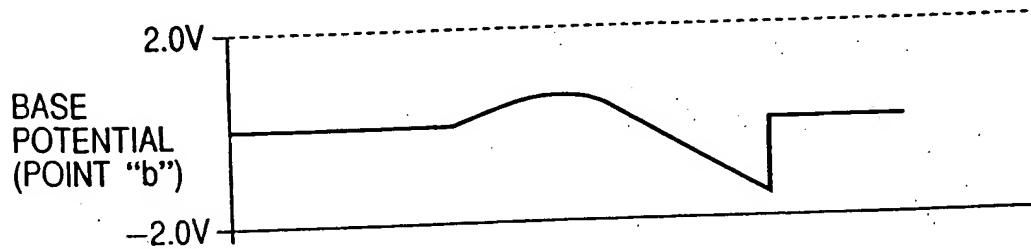


FIG. 36C

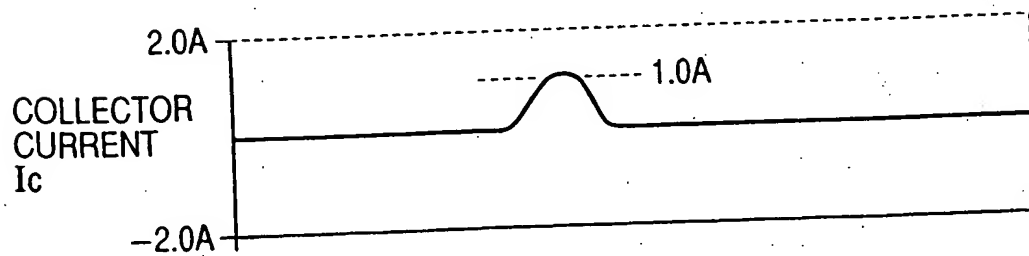


FIG. 36D

